The Improved Intrinsic Stability of CdTe Polycrystalline Thin Film Devices

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ABSTRACT

A systems-driven approach linking upstream solar cell device fabrication history with downstream performance and stability has been applied to CdS/CdTe small-area device research. The best resulting initial performance (using thinner CdS, thicker CdTe, no oxygen during VCC, and the use of NP etch) was shown to simultaneously correlate with poor stability. Increasing the CdS layer thickness significantly improved stability at only a slight decrease in overall performance. It was also determined that cell perimeter effects can accelerate degradation in these devices. A "margined" contact significantly reduces the contribution of edge shunting to degradation, and thus yields a more accurate determination of the intrinsic stability. Pspice discrete element models demonstrate how spatially localized defects can effectively dominate degradation. Mitigation of *extrinsic* shunting improved stabilized efficiency degradation levels (SEDL) to near 20% in 100ºC tests. Further process optimization to reduce *intrinsic* effects improved SEDL to better than 10% at the same stress temperatures and times.

1. Objectives

Our objective during the course of this work was to implement an efficient infrastructure for correlating intrinsic stability with performance and fabrication metrics associated with a variety of NREL-developed, thin-film polycrystalline device technologies.

2. Technical Approach

Systems-driven methodology demands the close linking of a myriad of thin-film fabrication parameters, characterization data, and performance and stability measurements. To manage this data efficiently, a network-based, relational database with automated data-entry and post-process analysis capability was implemented. A stress-test system, capable of uniformly heating a large number of different CdTe devices under calibrated, 1-sun illumination was constructed. Cells were stressed under open-circuit conditions at temperatures of 100ºC. The percent change in device current-voltage (J-V) performance relative to it's initial value as a function of stress time and processing was used to generate various standard least-squares regression models. These models were then used to statistically analyze and optimize interactions between processing and stability. So-called "baseline" determinations of stability were performed on devices processed under "normal" growth and fabrication conditions.

3. Results and Accomplishments

Prior open-circuit, 1-2 sun, 100ºC stress tests, used to determine the intrinsic stability of NREL-made CdS/CdTe devices, used a device fabrication structure where the paste backcontact layers were separated from the front tin-oxide contact by only a few microns of CdS and CdTe [1]. This process is highly sensitive to the edge definition and scraping technique. In this research, a new "margined" contact definition approach, shown in Fig. 1, was used in which a ~1 mm margin of CdTe was placed between the Ag-metal backcontact and the front, SnO_2 contact.

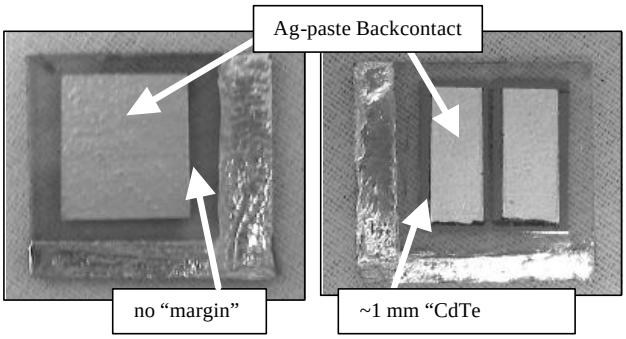

Figure 1. Conventional "no-margin" and new "margined" approach to backcontact definition.

A comparison of the baseline stability of CdS/CdTe devices using these backcontact structures is shown in Fig. 2. The degradation rates exhibited by the margined (X) and no-margined (O) cells are distinctly different. Degradation for the margined cells was tightly grouped and leveled off fairly quickly during the test achieving a SEDL near 20% within approximately 300 hours of testing. For the NP-etched, no-margined cells, much larger variations in degradation rates were observed. In no-margined cells, efficiency did not stabilize and reached a degraded level of between 60-80% of their initial performance by the conclusion of the test. The asymptotic approach of the margined-cell to a stabilized level reflects some finite amount of reaction product involved in the degradation. Similar stabilized behavior has been reported by Enzenroth et al.[2].

The rapid degradation demonstrated in Fig. 2 by baseline non-margined cells can be replicated in margined cells if the

CdS window layer thickness is reduced. In a large (48 device) orthogonal experiment designed to study the effect of CdS and CdTe layer thickness, VCC oxygen ambient, and the use of NP etching on stability, we observed such rapid degradation only in cases where CdS film growth time was decreased from the nominal value of 37m to 34m. A least-squares regression model generated from the remaining data showed excellent correlation with experiment.

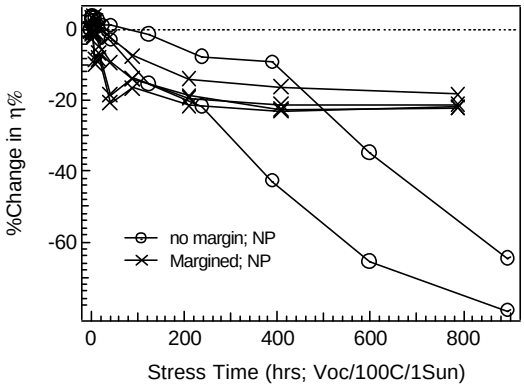

Figure 2. Comparison of margined and non-margined cell structures

This model accurately predicted that the highest initial performance obtained using the thinnest (34 min. deposition) CdS layers, thickest (11 um) CdTe films, 0% VCC oxygen ambient, and the use of NP etching prior to contacting. This fabrication scheme demonstrated low and non-stabilized stability (predicted and actual η% degradation levels of 49.6 and 87.0% respectively). The model also predicted a large improvement in SEDL by increasing CdS layer thickness (41 min. deposition level). ***Predicted and actual SEDLs of 14.6% and 8.3% were the result of this optimization***. This change resulted in only a slight decrease in the initial performance (modeled and actual η% drops of 12.9% to 12.6%, and 13.1% to 12.5%, respectively) demonstrating how stability can be improved in small-area devices with minor impact on performance.

Rapid degradation similar to that shown in Figure 2 and observed in CdS/CdTe devices using thin CdS window layers was determined to be spatially rather than uniformly dependent across the junction area. Infrared thermography images of a degraded cell (margined; thin CdS) are shown in Fig. 3.

This image was taken at 1.2 volts forward-bias (6.0 mA). The margin boundary is indicated by the dashed rectangle. Hot spots appear to be distributed in non-uniform fashion both within the cell interior as well as at the bottom-right corner. When the latter corner was removed by edge redefinition, a large increase in performance was regained. The performance of this cell initially, after degradation, and upon redefinition of the localized corner defect was 13.1%, 1.3%, and 11.6% respectively.

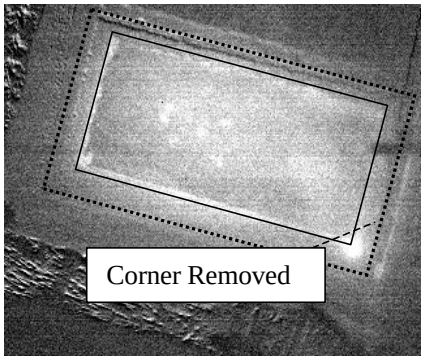

Figure 3. IR image of degraded cell

A 10-diode Pspice model was used to extract diode quality factor A, reverse-saturation current J_o (mA/cm^2), and series, Rs, and shunt, R_{sh}, resistance (ohms*cm^2) through curve-fitting experimental JV data (Table 1). Also shown in this table is the traditional 1-diode circuit equivalent model fit.

Table 1. One and Ten Diode Degradation Model Fits

Condition	Model	Jo	A	Rs	Rsh
unstressed	1-diode lumped	1.7e-8	2.2	0.54	430
unstressed	10-diode (unstressed)	1e-11	1.7	0.4	4.5k
stressed	1 weak diode 9 stressed diodes	2.0e-3 1e-10	2.2 1.8	0.2 0.8	20 4.5k
Corner removed	9 stressed diodes	1e-10	1.8	0.8	4.5k

These models show extrinsic degradation as being spatially related to localized combinations of excessive shunting and weak-diode formation. Interestingly, the distributed diode model generates more reasonable values of J_o and A in these devices when compared to conventional 1-diode "lumped" equivalent-circuit models.

4. Conclusions

Degradation studies of CdS/CdTe devices can be dominated by extrinsic effects yielding an inaccurate assessment of intrinsic stability. The latter can be improved by judicious choice of fabrication procedures.

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